

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)
2. (Canceled)
3. (Currently amended) ~~The method of claim 1 including~~ A method for applying test patterns to scan chains in a circuit-under-test, the method comprising:
providing a compressed test pattern of bits;
decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided;
applying the decompressed test pattern to scan chains of the circuit-under-test; and
providing the compressed test pattern through input channels to a circuit-under-test, the number of test channels being fewer than the number of scan chains to which the decompressed pattern is applied.
4. (Currently amended) ~~The method of claim 1~~ A method for applying test patterns to scan chains in a circuit-under-test, the method comprising:
providing a compressed test pattern of bits;
decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided; and
applying the decompressed test pattern to scan chains of the circuit-under-test,
wherein providing the compressed test pattern, decompressing the compressed test pattern, and applying the decompressed pattern are performed synchronously at a same clock rate.

5. (Currently amended) ~~The method of claim 1~~ A method for applying test patterns to scan chains in a circuit-under-test, the method comprising:
providing a compressed test pattern of bits;
decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided; and
applying the decompressed test pattern to scan chains of the circuit-under-test,
wherein the compressed test pattern is provided at a lower clock rate and the compressed test pattern is decompressed and applied synchronously at a higher clock rate.

6. (Currently amended) ~~The method of claim 1~~ A method for applying test patterns to scan chains in a circuit-under-test, the method comprising:
providing a compressed test pattern of bits;
decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided; and
applying the decompressed test pattern to scan chains of the circuit-under-test,
wherein the compressed pattern is provided and decompressed at a higher clock rate and the decompressed pattern is applied synchronously at a lower clock rate.

7. (Currently amended) ~~The method of claim 1~~ A method for applying test patterns to scan chains in a circuit-under-test, the method comprising:
providing a compressed test pattern of bits;
decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided; and
applying the decompressed test pattern to scan chains of the circuit-under-test,
wherein decompressing the compressed test pattern comprises generating during a time period a greater number of decompressed test pattern bits than the number of compressed test pattern bits provided during the same time period.

8. (Original) The method of claim 7 wherein the greater number of bits is generated by providing a greater number of outputs for decompressed test pattern bits than the number of inputs to which the compressed test pattern bits are provided.

9. (Original) The method of claim 7 wherein the greater number of bits is generated by generating the decompressed test pattern bits at a higher clock rate than the clock rate at which the compressed test pattern bits are provided.

10. (Currently amended) ~~The method of claim 1~~ A method for applying test patterns to scan chains in a circuit-under-test, the method comprising:

providing a compressed test pattern of bits;

decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided; and

applying the decompressed test pattern to scan chains of the circuit-under-test,

wherein applying the decompressed test pattern to the scan chains comprises applying during a time period a greater number of decompressed test pattern bits to the scan chains than the number of compressed test pattern provided during the same time period.

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Currently amended) The method of claim ~~13~~ 3 wherein decompressing the compressed test pattern comprises generating one or more bits of the decompressed pattern by logically combining two or more bits of the compressed test pattern, and wherein logically combining two or more bits of the compressed test pattern comprises combining the bits with an XNOR operation.

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Currently amended) ~~The circuit of claim 26~~ A circuit comprising:
a decompressor adapted to receive a compressed test pattern of bits and decompress the
test pattern into a decompressed test pattern of bits as the compressed test pattern is being
received;
circuit logic; and
scan chains for testing the circuit logic, the scan chains coupled to the decompressor and
adapted to receive the decompressed test pattern,
wherein the decompressor comprises a linear finite state machine adapted to receive the
compressed test pattern, wherein the decompressor includes a phase shifter coupled between the

linear finite state machine and the scan chains, and wherein the phase shifter comprises an array of XNOR gates.

29. (Canceled)

30. (Canceled)

31. (Canceled)

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (Canceled)

36. (Canceled)

37. (Canceled)

38. (Canceled)

39. (Canceled)

40. (Canceled)

41. (Currently amended) ~~The method of claim 1 further including~~ A method for applying test patterns to scan chains in a circuit-under-test, the method comprising: providing a compressed test pattern of bits;

decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided;

applying the decompressed test pattern to scan chains of the circuit-under-test; and
loading an intermediate register with the compressed test pattern, the intermediate register positioned between a decompressor, which is performing the decompressing, and automated test equipment which is providing the compressed test pattern.

42. (Currently amended) ~~The circuit of claim 22 further including~~ A circuit comprising:
a decompressor adapted to receive a compressed test pattern of bits and decompress the test pattern into a decompressed test pattern of bits as the compressed test pattern is being received;

circuit logic;
scan chains for testing the circuit logic, the scan chains coupled to the decompressor and adapted to receive the decompressed test pattern; and

automated test equipment coupled externally to the circuit and an intermediate register coupled between the automated test equipment and the ~~decompression~~ decompressor.

43. (Previously presented) The circuit of claim 42, wherein the intermediate register receives compressed test patterns from the automated test equipment and provides the compressed test patterns to the decompressor.

44. (Canceled)

45. (Currently amended) ~~The circuit of claim 30, further including~~ A circuit comprising:
a decompressor adapted to receive a compressed test pattern of bits and decompress the test pattern into a decompressed test pattern of bits, the decompressor having a plurality of input channels and a plurality of outputs, the input channels receiving in parallel the bits of the compressed test pattern;

circuit logic;
scan chains for testing the circuit logic, the scan chains coupled to the outputs of the decompressor and adapted to receive the decompressed test pattern in parallel; and

automated test equipment coupled externally to the circuit and an intermediate register positioned between the automated test equipment and the decompressor.

46. (Currently amended) ~~The circuit of claim 32, further including~~ A circuit comprising:
a linear finite state machine having input logic gates adapted to logically combine bits
stored within the machine with bits received from a compressed test pattern, the state machine
generating therefrom a series of bits;

a phase shifter coupled to the linear finite state machine, the phase shifter adapted to
logically combine two or more bits generated by the linear finite state machine to produce a
decompressed pattern of bits;

scan chains coupled to the phase shifter and adapted to receive therefrom the
decompressed test pattern; and

automated test equipment coupled externally to the circuit and an intermediate register positioned between the automated test equipment and the linear finite state machine.

47. (Currently amended) ~~The circuit of claim 32,~~ A circuit comprising:
a linear finite state machine having input logic gates adapted to logically combine bits
stored within the machine with bits received from a compressed test pattern, the state machine
generating therefrom a series of bits;

a phase shifter coupled to the linear finite state machine, the phase shifter adapted to
logically combine two or more bits generated by the linear finite state machine to produce a
decompressed pattern of bits; and

scan chains coupled to the phase shifter and adapted to receive therefrom the
decompressed test pattern,

wherein the bits of the compressed test pattern are received while the decompressed pattern of bits are produced.

48. (Canceled)

49. (Currently amended) ~~The circuit of claim 32,~~ A circuit comprising:

a linear finite state machine having input logic gates adapted to logically combine bits stored within the machine with bits received from a compressed test pattern, the state machine generating therefrom a series of bits;

a phase shifter coupled to the linear finite state machine, the phase shifter adapted to logically combine two or more bits generated by the linear finite state machine to produce a decompressed pattern of bits; and

scan chains coupled to the phase shifter and adapted to receive therefrom the decompressed test pattern,

wherein the linear state machine receives bits of the compressed test pattern substantially concurrent with the phase shifter producing a decompressed pattern of bits.

50. (Canceled)

51. (Canceled)

52. (Canceled)

53. (Canceled)

54. (Canceled)

55. (Canceled)

56. (Canceled)

57. (Canceled)

58. (Canceled)

59. (Canceled)

60. (Canceled)

61. (New) The method of claim 3, wherein decompressing the compressed test pattern comprises generating one or more bits of the decompressed pattern by logically combining two or more bits of the compressed test pattern.

62. (New) The method of claim 61, wherein logically combining two or more bits of the compressed test pattern comprises combining the bits with an XOR operation.

63. (New) The method of claim 3, wherein the compressed test pattern is a deterministic test pattern.

64. (New) The method of claim 3, wherein the providing and decompressing occur within the circuit-under-test.

65. (New) The method of claim 4, wherein decompressing the compressed test pattern comprises generating one or more bits of the decompressed pattern by logically combining two or more bits of the compressed test pattern.

66. (New) The method of claim 65, wherein logically combining two or more bits of the compressed test pattern comprises combining the bits with an XOR operation.

67. (New) The method of claim 4, wherein the compressed test pattern is a deterministic test pattern.

68. (New) The method of claim 4, wherein the providing and decompressing occur within the circuit-under-test.

69. (New) The method of claim 5, wherein decompressing the compressed test pattern comprises generating one or more bits of the decompressed pattern by logically combining two or more bits of the compressed test pattern.

70. (New) The method of claim 69, wherein logically combining two or more bits of the compressed test pattern comprises combining the bits with an XOR operation.

71. (New) The method of claim 5, wherein the compressed test pattern is a deterministic test pattern.

72. (New) The method of claim 5, wherein the providing and decompressing occur within the circuit-under-test.

73. (New) The method of claim 7, wherein decompressing the compressed test pattern comprises generating one or more bits of the decompressed pattern by logically combining two or more bits of the compressed test pattern.

74. (New) The method of claim 73, wherein logically combining two or more bits of the compressed test pattern comprises combining the bits with an XOR operation.

75. (New) The method of claim 7, wherein the compressed test pattern is a deterministic test pattern.

76. (New) The method of claim 7, wherein the providing and decompressing occur within the circuit-under-test.

77. (New) The method of claim 10, wherein decompressing the compressed test pattern comprises generating one or more bits of the decompressed pattern by logically combining two or more bits of the compressed test pattern.

78. (New) The method of claim 77, wherein logically combining two or more bits of the compressed test pattern comprises combining the bits with an XOR operation.

79. (New) The method of claim 10, wherein the compressed test pattern is a deterministic test pattern.

80. (New) The method of claim 10, wherein the providing and decompressing occur within the circuit-under-test.

81. (New) The circuit of claim 47, wherein the number of scan chains is greater than the number of input channels.

82. (New) The circuit of claim 49, wherein the number of scan chains is greater than the number of input channels.